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Attorney Docket No. : MICRON.003C1
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For : STREAMLINED FIELD ISOLATION
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Attorney : James B. Bear
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I hereby certify that the accompanying

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ATTENTION: APPLICATION BRANCH

Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): **Pierre C. Fazan, Viju K. Matthews and Nanseng Jeng**

For: **STREAMLINED FIELD ISOLATION PROCESS**

Enclosed are:

- (X) 4 sheet(s) of drawings.
- (X) This application is a continuation of prior application 08/519,451, filed August 25, 1995.
- (X) A copy of Declaration from the prior application is enclosed.
- (X) A copy of power of attorney form and copy of assignment from the prior application is enclosed.
- () Deletion of Inventors: Signed statement attached requesting deletion of person(s) not inventor(s) in the present application.
- (X) Incorporation by Reference. The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
- (X) Return prepaid postcard.

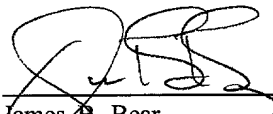
CLAIMS AS FILED

FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE
Basic Fee			\$790	\$790
Total Claims	10 - 20 =	0 ×	\$22	\$0.00
Independent Claims	3 - 3 =	0 ×	\$82	\$0.00
If application contains any multiple dependent claims(s), then add			\$270	\$0.00
TOTAL FILING FEE				\$790

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(X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Account No. 11-1410. A duplicate copy of this sheet is enclosed.

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STREAMLINED FIELD ISOLATION PROCESS

Field of the Invention

The invention relates generally to silicon integrated circuit fabrication. In particular, the invention pertains to the device isolation processes involving the local oxidation of silicon.

Background of the Invention

Implementing electric circuits in an integrated process involves connecting isolated devices through specific electrical paths. In silicon ultra large scale integration, effective device isolation becomes increasingly important as device dimensions become smaller and packing density rises.

In conventional Metal-Oxide-Silicon (MOS) device fabrication, device isolation is often implemented by means of recessed or semi-recessed silicon dioxide (SiO_2 or "oxide") regions in the non-active or field areas of the silicon substrate. This so-called Local Oxidation of Silicon (LOCOS) has become the most widely used isolation technology. In various forms, it remains the technique of choice for MOS device isolation.

A basic LOCOS process begins with the formation of a relatively thin (20-60 nm) pad-oxide layer over substantially an entire clean silicon (Si) wafer. Following the pad-oxide deposition, a silicon nitride (Si_3N_4 or "nitride") layer of about 100-200 nm thick is deposited. Subsequently, the wafer is masked and the nitride/pad-oxide is etched to define the active regions. The exposed regions are the inactive or field regions wherein the field oxide is grown. Prior to oxide growth, optional dopant implants may be carried out to create channel-stops located beneath the field oxide. The field oxide is typically thermally grown at about atmospheric pressure by means of wet oxidation, at temperatures of about 1000°C for 2-4 hours, resulting in oxide thicknesses in the range of 0.3-1.0 μm . Dry oxidation is usually not preferred because of the generally low oxidation rate which adds considerably to process throughput.

Even though the oxide grows substantially only within the regions defined by the masking nitride, some oxidant may diffuse laterally causing excess oxide to grow under the edges of the nitride mask, often forming a so-called "bird's beak" effect.

The bird's beak presents several problems for device isolation. Modifications of the basic LOCOS isolation process have succeeded in reducing the bird's beak considerably.

During the growth of the field oxide, another phenomenon occurs that causes defects in the structure, which later become detrimental to the thin gate oxide. Kooi, et al. (J. Electrochem. Soc., vol. 123, pp. 1117, 1976), discovered that a thin layer of silicon nitride can form on the silicon surface at the pad-oxide/silicon interface as a result of the reaction of ammonia (NH_3) and silicon. The ammonia is generated from the reaction between water vapor (H_2O) and the masking nitride during the field-oxidation step. The ammonia diffuses through the pad oxide and reacts with the silicon substrate to form silicon nitride spots or ribbons, sometimes called the *white ribbon* effect. Subsequently, when the gate oxide is grown, the growth rate becomes impeded at the locations where the silicon nitride has formed. The gate oxide is thus thinner at these locations than elsewhere, causing low-voltage breakdown of the gate oxide. One common way to eliminate this problem is to grow a "sacrificial" oxide layer after etching the masking nitride and pad-oxide layers. The sacrificial oxide is then removed before growing the final gate oxide. Clearly, however, the additional processes involved for eliminating the Kooi effect adds to the cost and complexity of ULSI fabrication.

Summary of the Invention

It is an object of the present invention to provide a field isolation process which obviates the need for sacrificial oxide growth and removal to eliminate parasitic silicon nitride inclusions. It is a further object of the present invention to provide a field oxidation process which prevents the formation of silicon nitride inclusions at the silicon/silicon dioxide interface. It is yet another object of the present invention to provide a field oxidation process which eliminates the use of hydrogen-containing oxidants, thereby preventing silicon nitride formation concurrent with the field oxide formation and achieve the requisite field oxide growth.

In accordance with one aspect of the present invention, a field isolation process comprises growing a field oxide region on a semiconductor wafer by means of a hydrogen-free oxidant. Preferably the oxidant comprises substantially only oxygen

and the field oxide process is preferably carried out at oxygen partial pressures greater than 10 atm and temperatures greater than about 900 °C.

In accordance with another aspect of the present invention, a method of growing a field oxide region on a semiconductor wafer comprises growing a first portion of the field oxide region by means of exposing a portion of the wafer to a first oxidizing ambient comprising water vapor. The field oxide region is completed by further exposing the portion of the wafer to a second oxidizing ambient comprising oxygen.

In accordance with yet another aspect of the present invention, a field isolation region on a semiconductor substrate is formed by a process comprised of exposing the field region of the semiconductor wafer to an oxidizing ambient comprising substantially only oxygen. More preferably, the isolation region is first exposed to an oxidizing ambient comprising at least in part water vapor, and subsequently exposed to the oxidizing ambient comprised of substantially only oxygen.

These as well as other objects and attributes of the present invention will become more fully apparent from the following description with reference to the accompanying drawings.

Brief Description of the Drawings

Figures 1A-1H is a schematic partial process flow illustrating a representative field isolation process and the accompanying Kooi effect.

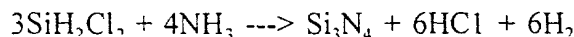
Figure 2A-2B is a schematic partial process flow illustrating a field oxide grown by high pressure oxidation.

Figure 3A-3C is a schematic partial process flow illustrating a field oxide with encapsulated parasitic nitride.

Detailed Description of the Invention

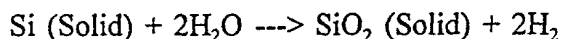
As shown in Figure 1A, an exemplary conventional LOCOS process begins by depositing a buffer or pad-oxide layer (SiO_2) 14 of about 20-60 nm thick on a clean surface of a silicon wafer 12. The pad-oxide provides a stress relief buffer between the silicon surface and an overlaying silicon nitride layer. As shown in Figure 1B, a layer of silicon nitride 16 of about 100-200 nm thick is deposited on the pad-oxide. Silicon nitride is typically deposited by a chemical vapor deposition (CVD) of

dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) at temperatures between 700°C and 800°C , according to the overall reaction:



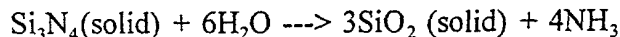
A photolithographic process is then used to define the active regions. A resist pattern is normally used to protect all of the areas where the active devices will be formed. The nitride layer is then dry etched and the pad-oxide is etched by either a wet-or-dry-chemical process. Figure 1C illustrates an exemplary structure resulting from the masking and etch process. After the mask and etch process, optional dopant implants may be formed in the field regions, creating a channel-stop 20, as shown in Figure 1D. The channel-stop 20 is intended to provide enhanced device isolation and is thus mentioned by way of example as a common practice in LOCOS process integration. Moreover, the channel-stop implant 20 may be performed in other ways, for example after field oxide growth. It will be appreciated that such channel-stop implant processes may be integrated in a variety of ways, and are optional in the context of the present invention.

The field oxide is thermally grown by means of wet oxidation according to the general formula:

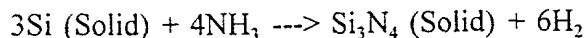


Typical field oxide layers 22 as shown in Figure 1E are grown to thicknesses of about 0.3 to $1.0\text{ }\mu\text{m}$. Wet oxidation is typically carried out at temperatures in the range of 900°C to 1200°C and oxidant partial pressures from about 0.2 to 25 atm. As a silicon oxidant, water vapor is conventionally preferable because of the generally high oxidation rate.

However, during growth of the field oxide 22, a parasitic inclusion of silicon nitride can form at the silicon/pad-oxide interface as a result of the reaction of released ammonia with silicon. Specifically, ammonia is released by the reaction of Si_3N_4 (Solid) and H_2O present during wet oxidation according to the approximate formula:



Ammonia released by the reaction diffuses through the SiO_2 pad-oxide layer and reacts with the silicon substantially at the Si/SiO_2 interface according to the general formula:



As shown in Figure 1E, the parasitic nitride inclusions 24 generally grow at the Si/SiO₂ interface adjacent to the field oxide 22. Subsequent nitride and pad-oxide etching processes leave the surface of the silicon substrate exposed for further processing. However, the nitride inclusions 24 are also present at the silicon surface, as illustrated in Figure 1F. Further processing is compromised by the presence of the nitride inclusions 24. For example, subsequent growth of a gate oxide layer requires a thin, high quality oxide having uniform thickness and composition. The nitride inclusions 24 cause the gate oxide to become thinner in these regions which ultimately contributes to device breakdowns. Thus, additional processing is needed to alleviate this problem.

As shown in Figure 1G, typically a sacrificial oxide layer 26 is grown over the silicon surface to an extent which substantially oxidizes the nitride inclusions 24. The sacrificial oxide 26 is then etched, leaving a silicon surface and field oxide 22 substantially free of the nitride inclusions 24, as illustrated in Figure 1H. The aforementioned sacrificial oxide growth and removal have, conventionally, been considered necessary process steps for alleviating the Kooi effect.

In accordance with the principles of the present invention, a preferred isolation process comprises utilizing a high pressure field oxidation (HiPox) process using an oxidant substantially free of hydrogen. In this respect, it is preferable to perform a field HiPox process using an oxidant such as oxygen (O₂) in place of H₂O. Performing the oxidation of silicon at high pressure significantly enhances the oxidation rate, thus compensating a possible lower oxidation rate of O₂ relative to that of H₂O. Performing a field oxidation using an oxidant, substantially free of hydrogen, such as substantially pure oxygen prevents formation of silicon nitride inclusions via the Kooi effect.

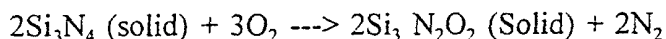
One embodiment of a preferred field oxidation process is illustrated in Figures 2A-2B. Figure 2A illustrates a wafer section processed up to the point of field oxidation. Previous processing steps may be substantially equivalent to that described in connection with Figures 1A-1D. As shown in Figure 2A, a starting structure may comprise the silicon substrate 12, pad-oxide layer 14, nitride mask 18 and optional channel-stop implant 20. Figure 2B illustrates the result of a high pressure field

oxidation using O₂ as the oxidant. The field oxide 20 is grown substantially similar to that described previously in connection with Figure 1E, except that the nitride inclusions 24 are eliminated.

A preferred HiPox process using O₂ follows the general formula:



It is possible that nitrogen (N₂) may be released in a possible accompanying reaction of O₂ with the masking nitride 18 according to the following approximate reaction or variations from stoichiometry thereof:



10 However, N₂ does not react significantly with the underlying silicon, as does the NH₃ released in the prior art field oxidation. A HiPox field oxidation is generally performed at partial pressures in the range of 5 atm to 30 atm, and in a temperature range of 900 °C to 1200 °C. Resulting oxidation rates may range from 2 nm/min. to 8 nm/min. Preferable HiPox processes are performed at O₂ partial pressures of about 15 25 atm, at 1000 °C resulting in oxidation rates of about 5 nm/min.

Having a field oxide substantially free of nitride inclusions 26 (Figure 1), allows subsequent processing without the need for sacrificial oxide growth as discussed in connection with Figures 1G and 1H.

Another preferred field oxidation process comprises a two-step operation, whereby an initial field oxide is grown by wet oxidation followed by a HiPox oxidation step. As shown in Figure 3A, a possible starting structure may comprise the result of prior processing steps as described in connection with Figures 1A-1D. As shown in Figure 3B, a first partial field oxide 28 is grown by wet oxidation, as previously described in connection with Figure 1E. The wet oxidation process, 20 however, produces residual nitride inclusions 30. A second field oxidation is then performed by HiPox using an O₂ oxidant. As shown in Figure 3C, the HiPox step substantially completes the field oxide 32, and grows an oxide which consumes the nitride inclusions 30. Since the nitride inclusions are no longer located at the Si/SiO₂ interface, their influence on subsequent processing steps is ameliorated. Advantages 25 of the present embodiment include use of the relatively inexpensive and efficient wet 30

oxidation to create a portion of the field oxide, minimizing the more expensive HiPox process and eliminating the need for the sacrificial oxide.

Although described above with reference to the preferred embodiments, modifications within the scope of the invention may be apparent to those skilled in the art, all such modifications are intended to be within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A field isolation process comprising growing a silicon dioxide field isolation region on a semiconductor wafer by means of a hydrogen-free oxidant.

2. The process of Claim 1 wherein the oxidant comprises substantially only oxygen.

3. The process of Claim 1, further comprising exposing the semiconductor wafer to the oxidant at an oxidant partial pressure greater than 5 atm.

4. The process of Claim 1, further comprising maintaining the semiconducting wafer at a temperature greater than 900 °C.

5. A method of growing a field oxide region on a semiconductor wafer comprising the steps of:

growing a first portion of the field oxide region by means of exposing a portion of the wafer to a first oxidizing ambient comprising water vapor; and

growing a second portion of the field oxide region by means of exposing the portion of the wafer to a second oxidizing ambient comprising oxygen.

6. The method of Claim 5, wherein the first oxidizing ambient is maintained at a temperature greater than 900 °C and a pressure greater than 5 atm.

7. The method of Claim 5, wherein the second oxidizing ambient is maintained at a temperature greater than 900 °C and pressure greater than 5 atm.

8. A field isolation region on a semiconductor wafer formed by a process comprising:

exposing a field region of the semiconductor wafer to an oxidizing ambient comprising substantially only oxygen.

9. The field isolation region of Claim 8, wherein the oxidizing ambient is maintained at a pressure greater than 5 atm and a temperature greater than 900 °C.

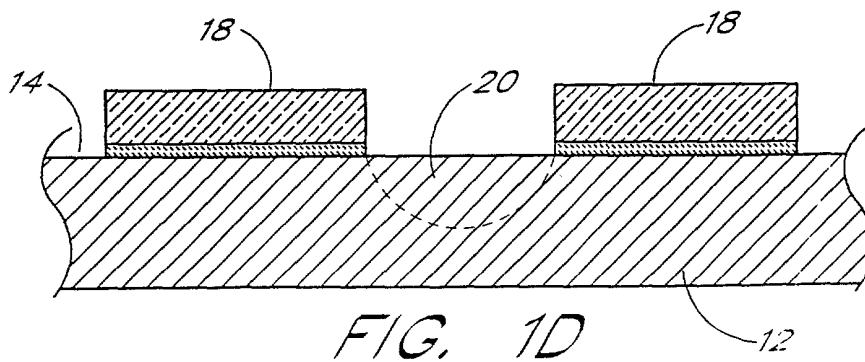
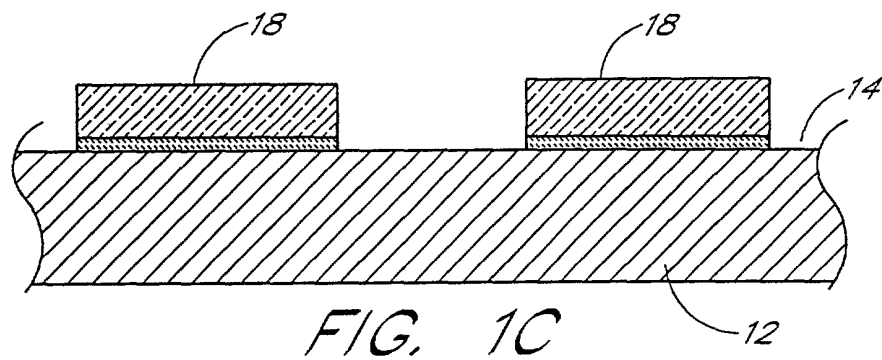
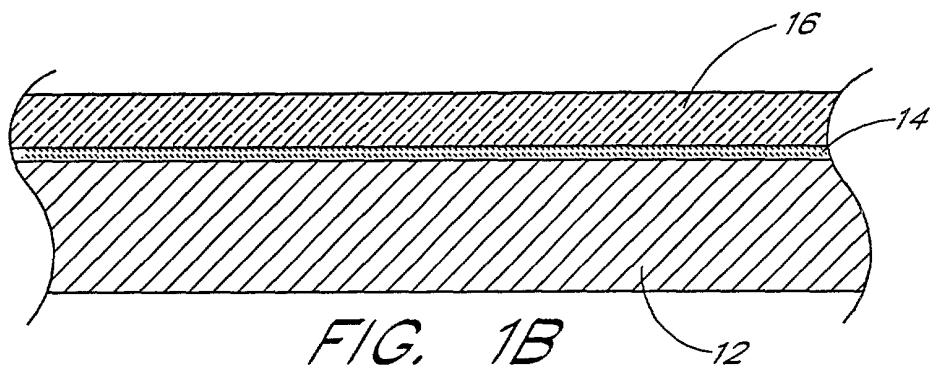
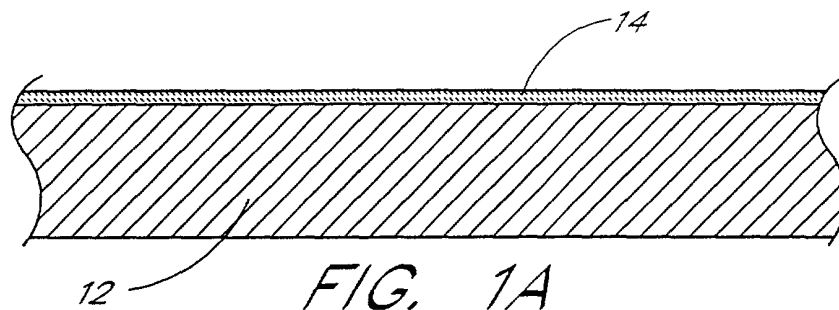
10. The field isolation region of Claim 8, further comprising exposing the field region to an oxidizing ambient comprising water vapor prior to exposing the field region to the oxidizing ambient comprising substantially only oxygen.

	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2
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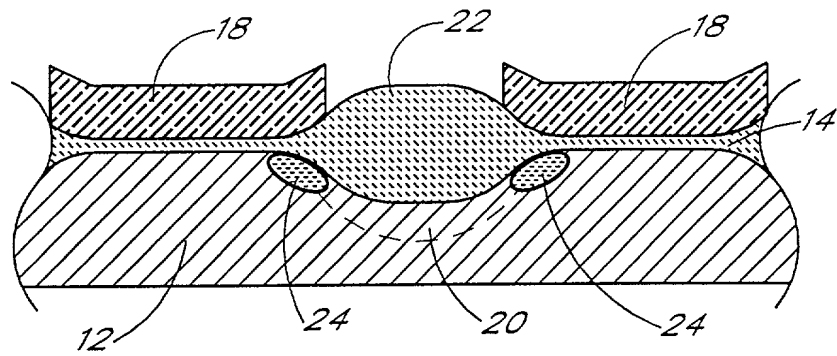


FIG. 1E

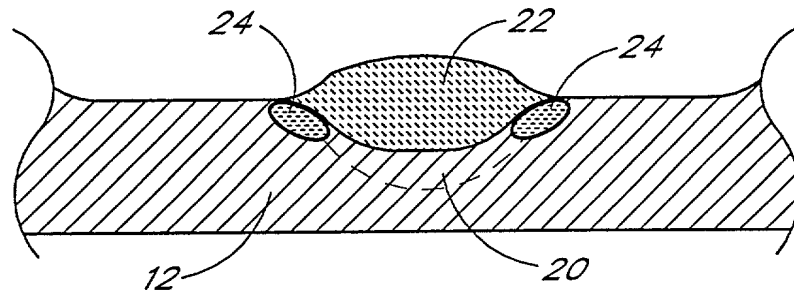


FIG. 1F

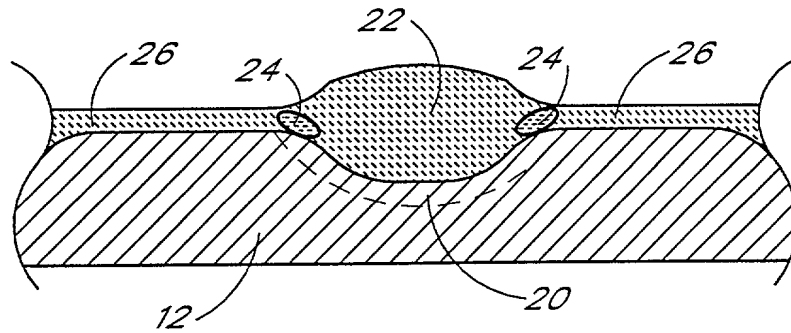


FIG. 1G

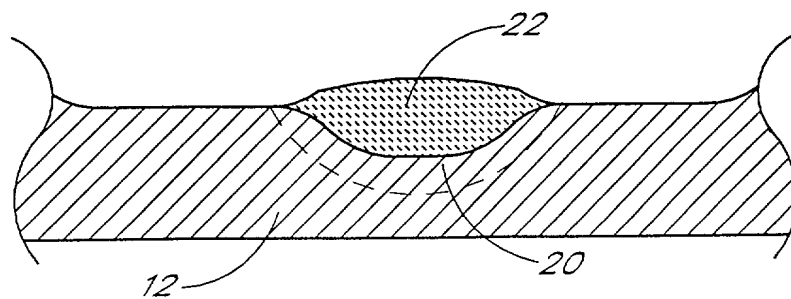


FIG. 1H

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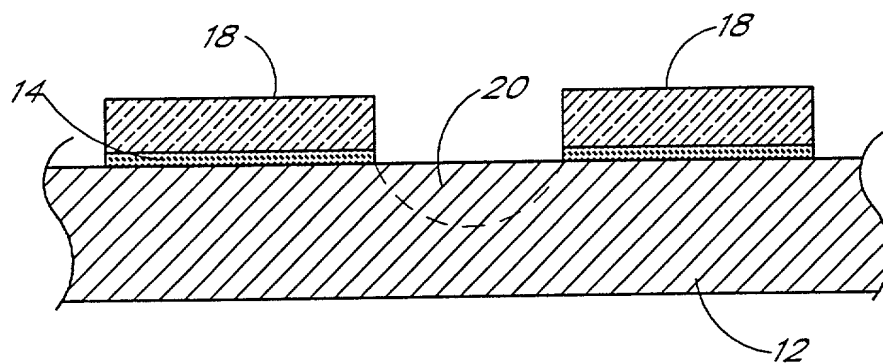


FIG. 2A

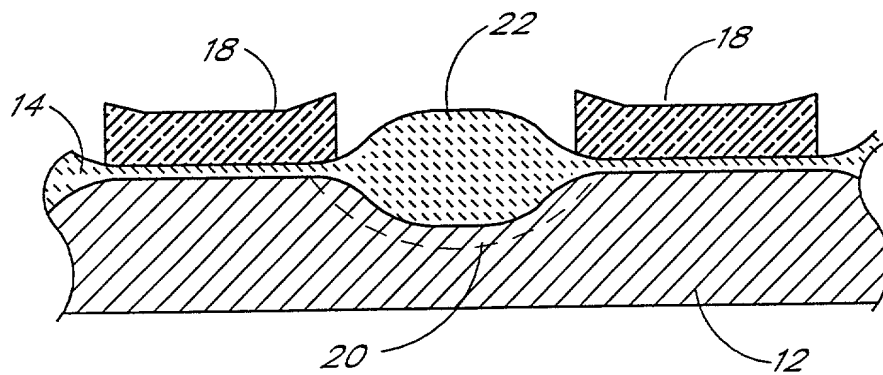


FIG. 2B

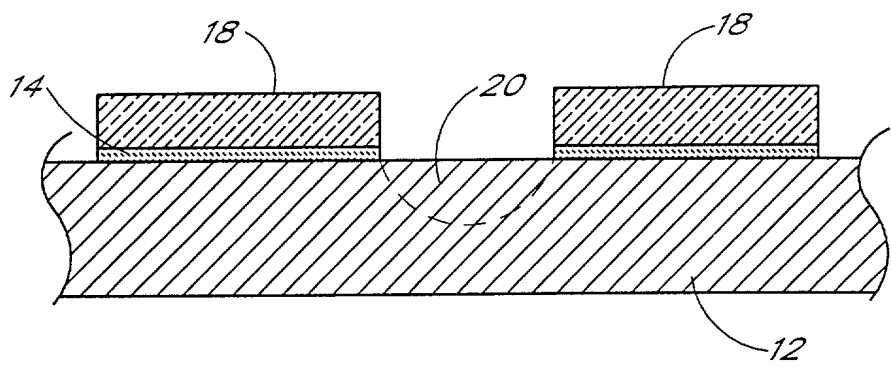


FIG. 3A

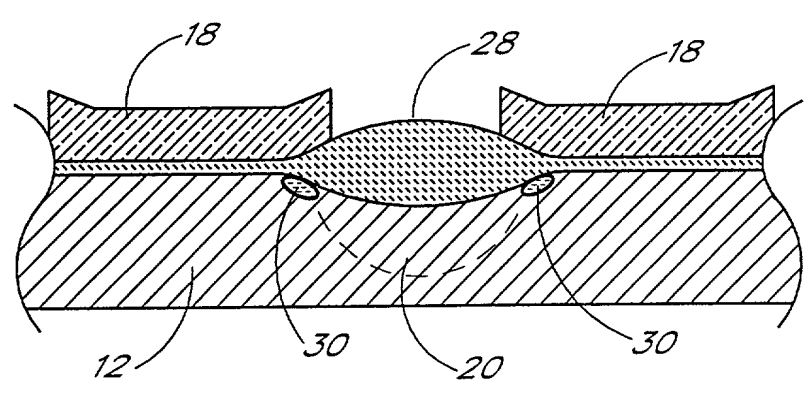


FIG. 3B

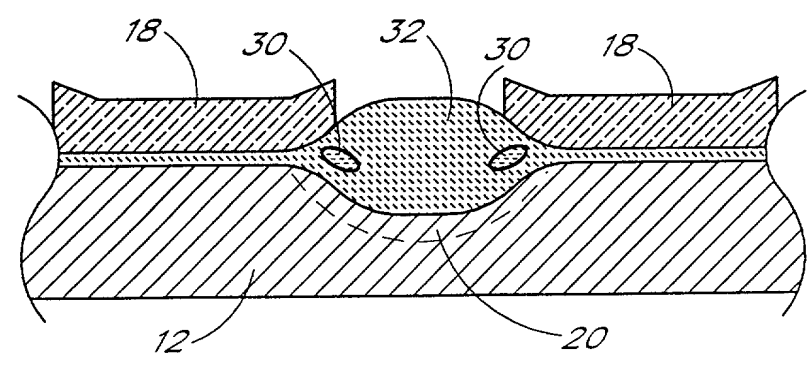


FIG. 3C

66160-846000

DECLARATION - USA PATENT APPLICATION

COPY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled STREAMLINED FIELD ISOLATION PROCESS; the specification of which is attached hereto;

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above;

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56;

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

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